

**Application Note** 

The Agilent i1000D diagnostics test set (DTS) provides boundary scan, on-board programming and general digital test in a desktop form factor that makes it easy to deploy for a flexible test strategy.



#### **Overview**

Boundary scan test is widely used in current production line test, to perform connectivity test, device programming, or disabling routine to protect devices under certain functional tests.

The Agilent i1000D in-circuit test (ICT) system is designed to serve general ICT purpose with costeffective press-down type fixtures without compromising the quality of test. The newly designed graphical user interface helps engineers to perform their routine tasks efficiently. The ease of use also means a shortening of the programming and debug time for mass production line test implementation.

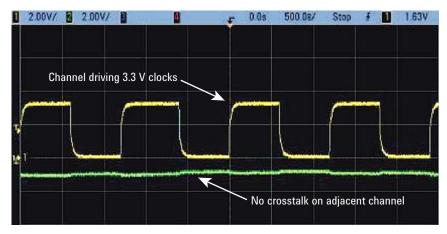


Figure 1. Signal integrity is ensured with the i1000D DTS anti-interference cabling design.

To meet the challenges and requirements of having a flexible test strategy for implementation at both the ICT and functional test stations, Agilent now provides a diagnostic application based on the i1000D ICT system - a desktop solution that allows easy and flexible deployment.

The i1000D diagnostics test set (DTS) uses the same hardware engine as the i1000D system in a stand-alone form factor, which can be easily used for off-line R&D validation or serve as an independent programming station for diagnostic functional tests.

The basic configuration of the DTS provides 64 independent digital drivers and receivers. Each channel can be assigned for different purpose. With the innovative anti-interference cabling design, the U9401B-D01 hardware supports superior test signal integrity, which ensures the stability of tests in long wiring environments.

### **Boundary Scan**

The i1000D DTS can easily perform boundary scan tests via the predefined test option interface.

The user can easily assign a test access port (TAP) to 4 to 5 channels, together with upstream device disabling requirement. After loading a correct boundary scan description language (BSDL) file, the boundary scan test program can be generated by simply selecting the test item in the boundary scan GUI.

Boundary integrity test, connect test, interconnect test, Device High Z, and Agilent's latest Cover-Extend Technology (CET) are now available in the boundary scan test predefined category.



Figure 2. Boundary scan GUI

#### **BSDL** Reader

With the easy-to-read BSDL interface, the test engineer can easily understand the content of the BSDL, and define which pin to be tested or removed from test list.

The i1000D DTS now supports the latest extest-toggle instruction, which is a customized boundary scan command for vectorless test without bed of nails.

Device											
						<ul> <li>Boundary Register</li> </ul>	C I	Extest	Toggle (	Cell .	
Device Name : b.	bod_b2_mobile			nce_P							
Instruction Register		Bou	and the second se	Registr		le	la di	In a		les el	
Instruction Length : 8			Skip		1.000	Port Name		Sale	Control Co	_	
Instruction Capture : 000	01001	1		0		STP_PCB_GPI034	bide	*	27	1	
Required Opcode :		2		1		SYS_RESETB	input	×	-1	-1	
BYPASS	11111111	3		2	BC_7	SATA3GP_GPI037	bidir	ĸ	28	1	
Sample/Preload	00000001	4		3	BC_7	INIT3_3/8	bidr	×	161	1	
EXTEST	00000000	5	1	4	BC_7	SDATAOUT0_GPI039	bide	×	27	1	
Optional Opcode :		6	1	5	BC_7	PCIECUKR028_GPI020	bide	×	28	1	
INTEST		7	1	6	BC_7	SATACLKREQB_GPI035	bide	*	28	1	
RUNBIST		8	1	7	BC.7	SPKR	bidr	×	23	1	
CLAMP		9	-	8	BC 7	SATAOGP GPI021	bide	*	28	1	
HIGHZ	00000011	10	-	9		POECLKRO18 GPID18	bide	*	27	1	
IDCODE	00000101	11	-	10		SLOAD GPI038	bide	2	27	1	
USERCODE	and the second se	12	-	11		A20GATE	incut	-	-1	4	
EXTEST_TOGGLE		13	-	12	_	SATALEDB	bide	-	58	1	
EXTEST_TRAIN		100	-	1.7	-		2.2.2	-	-1	- i - i	
EXTEST_PULSE		14		13		RCINB	input	*		-1	
		15	V	14		SATA1GP_GPI019	bidr	*	27	1	
Idcode Register	Formation of the local division of the local	16	_	15		SDATAOUT1_GPI048	bide	×	27	1	
4-bit Version :		17		16		SCLOCK_GPI022	bidr	×	27	1	
16-bit Part Number :		18		17	BC_7	SATA2GP_GPI036	bide	×	29	1	
11-bit Manufacturer ID :		1									
Mandatory LSB :	p.	Bo	andary	Length	: 531	Total Skip Cel	: 10				

Figure 3. User-friendly BSDL Reader

# Cover-Extend Technology (Optional)

Agilent's award winning Cover-Extend Technology (CET) is now a supported option on the U9401B-D02. CET extends test coverage from boundary scan devices to adjacent devices with the industry's popular vectorless test solution, VTEP.

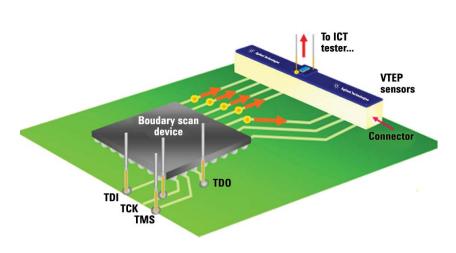


Figure 4. Diagrammatic representation of Cover-Extend Technology.

## On-Board Programming (I<sup>2</sup>C and SPI)

With the 64 independent digital drivers and receivers, the i1000D DTS can perform on-board programming.

I<sup>2</sup>C and SPI, are pre-defined formats in the software interface. The engineer can easily arrange the programming by selecting the device from the ready-to-use list. If the device is not in the list, it can be created by the 'LIB' creation tool.

# Support for VCL, PCF Library

Many Agilent i3070/3070 and i1000D ICT programmers are familiar with two digital test library formats, called "VCL" and "PCF" libraries.

The i1000D DTS supports any customized programming as long as there is an associated VCL or PCF library.

## **Flexible Digital Test**

U9401B-D01 supports simple digital tests like TTL, complex tests like XOR Tree Test or any digital test defined by VCL/PCF test, with H02 extension options. A total of 128 digital channels can be used.

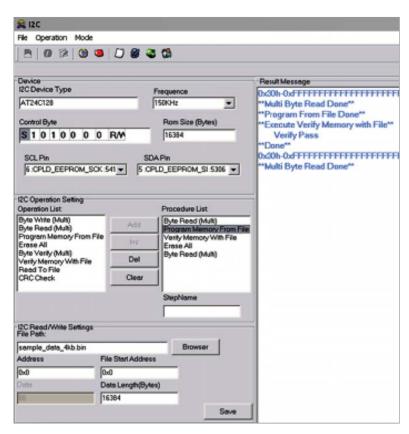


Figure 5. I<sup>2</sup>C,SPI OBP interface .

IC Port Nome	Manufacturer	Instruction (Hex. 0"FP)
Atmel AT25128A		Write Enable (Hex)
Protocol	Rom Type	105
SPI 💌	Flash Rom 💌	White Disable (Hex)
Device ID (Hex)	Rom Size (Bytes)	E4
None	16304 Byte 💌	Feed Status Register (Hex)
Address Length (Bits)	Page Size (Bytes)	IDS
16 💌	64	White Status Register (Hex)
SPI Status Register		En land
Bit7 (B+But		Pend Data (Hex)
	B	61
Ready Status (Hex. 0"FF)	Busy Bit Position (0"7)	Write Data (Hex)
0	jo	fitz
		Sector Erase (Hex)
		None
		Block Erase (Her)
		None
		Chip Erase (Her)
		Pione
		Read Device ID (Hex)
		None
Time Byte Write Time (us)	Page Write Time (us)	Need to input Address
0	5000	AAI Word Phogram (Nex)
Sector Erose Time (ms) Sk.En	ase Time (ms) ip Erose Time (ms)	P
0 0	0	

Figure 6. I<sup>2</sup>C and SPI library generator

### Software Integration

When the customer needs to integrate boundary scan tests into a functional test station, the programmer can use industry-standard SCPI interface and the Agilent I/O library to integrate the i1000D DTS as part of the required functional test.

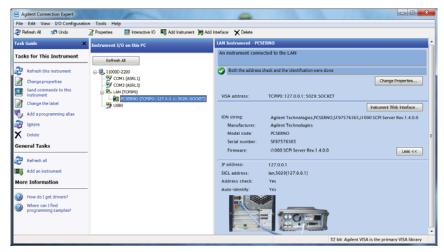


Figure 7. SCPI and Agilent I/O Library.

## Signal Layout

Half of the pins are reserved for ground. This is to ensure minimum cross talk among signals. Twisted pair wiring is highly recommended in any cable extension, thus, good signal integrity can be expected.

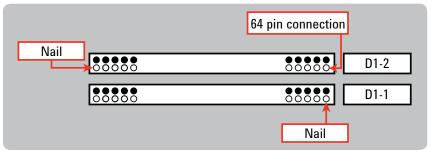


Figure 8. Signal layout in cable connection.

## Specifications for i1000D Diagnostic Test Set

	050
Max node count	256
Max digital driver/receiver channels	128
SCPI Command Support	Yes, thru LAN
External power supply control	Yes, thru Agilent IO Library
Agilent VTEP 2.0 Powered	Yes
On Board Programming	Yes
Boundary Scan	Yes, native with interconnect capabilities
Digital Test Library Support	Agilent VCL
Analog component test	Resistors, Capacitors, Inductors, Diodes, FET, and Jumpers.
Voltage measurement	Max 100V
Frequency measurement	200Mhz, 12 sets, with frequency mux card
Digital Driver/Receiver characteristics	
Mutiplexing	1:1, Unmuxed
Per-pin Programmable receiver	0 to 4.85 V
Per-pin Programmable driver	0 to 5 V
Max sink current	Peak 500 mA
Max source current	Peak 500 mA
Pattern rate	Max 2 MPS
Programmable vector cycle	Programmable
Programmable vector cycle resolution	50 ns
Programmable receive delay	Programmable
Programmable receive delay resolution	10 ns

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